UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/614,243	07/08/2003	Tohru Ueda	829-611	6228

23117 7590 12/14/2004

NIXON & VANDERHYE, PC
1100 N GLEBE ROAD
8TH FLOOR
ARLINGTON, VA 22201-4714

EXAMINER	
AKKAPEDDI, PRASAD R	

ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 12/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/614,243	UEDA ET AL.	
	Examiner	Art Unit	
	Prasad R Akkapeddi	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-24 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-24 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 08 July 2003 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 07/08/2003 (2).
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-3, 5 and 7 are rejected under 35 U.S.C. 102(b) as being anticipated by Hirata (U.S.Patent No. 5,811,866).

As to claim 1: Hirata discloses an active matrix board (or substrate) for use in liquid crystal display unit (col. 1, lines 6-7). Since Hirata teaches that the board is used in liquid crystal display unit, the counter substrate and a liquid crystal layer interposed between the active matrix substrate and the counter substrate are inherent. Hirata also teaches that the active matrix substrate includes a plate (1), a thin film transistor (2) and a light shield layer (7) for covering at least a portion of a side surface of the thin film transistor (Fig. 5). Note that the light shield layer (7) not only covers the top surface of the thin film transistor (TFT) but also some side portion of the TFT. In addition, the source electrode (4 in Fig. 4) made out of aluminum film covers the side of the TFT. Since, the source electrode is made out of aluminum, will also block the light to the TFT entering from the side of TFT. Hence, both the elements 7 and the source electrode (4) will act like side light shielding layers, which will satisfy the recited limitation.

As to claims 2 and 3: Hirata teaches a gate electrode region, a source electrode (4), a drain electrode (5), a pixel electrode (3). The specific structure of the TFT having a gate line and a semiconductor layer are inherent in the structure of the transistor (see Hashimoto reference cited below col. 1, lines 27-55).

As to claim 5: Hirata discloses a lower light shielding layer (11) provided below the TFT.

AS to claim 7: Hirata discloses an upper light shielding layer (7) that is provided on the TFT.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 4, 6, 8, 9 and 16-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirata in view of Sato (U.S.Patent No. 5,506,165).

As to claim 4: Hirata does not disclose an insulating layer on the substrate having a stepped portion and a light shielding layer along the side wall of the stepped portion of the insulating layer.

Sato in disclosing a liquid crystal display panel discloses a poly silicon layer (2), an insulating layer (3) where one can see the stepped portions in

Fig. 3 (d), an aluminum layer (10) which acts like a light shielding layer (due to the metallic nature of the layer), and at the stepped portions of the insulating layer.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to adapt the insulating layer and the light shielding layer along the stepped portions as disclosed by Sato to the device of Hirata to prevent breakdown in the drain of the thin film transistor (col. 2, lines 15-20).

As to claim 6, 8 and 9: Sato teaches that the light shield layer (10) contacts the poly silicon layer (also acts like a light shield in the visible wavelength region) through the contact hole as shown in Fig. 3(d) (col. 6, lines 14-16), as recited in the instant claim 6; and since the light shield layer (10) covers the entire TFT region, it is obvious to one having an ordinary skill in the art at the time invention was made to assess that the light shield layer (10) also covers the side surface of the gate and signal lines, as recited in instant claims 8 and 9.

As to claims 16-17: Hirata teaches that the top, side and bottom light shield layers are made of metal such as aluminum (col. 1, line 58) and in addition Sato teaches that the top and side light shield layer is made of aluminum and the bottom light shield layer (2) is poly silicon (col.4, lines 24-25).

5. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hirata and Sato as applied to claim1 above, and further in view of Hashimoto et al. (Hashimoto) (U.S.Patent No. 6,587,165).

As to claim 18: Hirata teaches a metal light shield layer and Sato teaches a metal and a poly silicon light shield layers.

However, neither Hirata nor Sato teaches a two layer combination.

Hashimoto in disclosing a thin film semiconductor device teaches two conductive layer combination for light shielding layers (col. 4, lines 41-46).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to adapt the two layers as the light shielding layer for maintaining a high image quality even under conditions with a large quantity of light coming from a light source (col. 2, lines 44-46).

6. Claims 10-15 rejected under 35 U.S.C. 103(a) as being unpatentable over Hirata in view of Hashimoto.

As to claims 10-15: Hashimoto in disclosing the prior art, discloses an auxiliary capacitance (13) and its connection to lower light shield layer (5), the TFT and the side light shielding layer (12 A or 12B) and the LDD region in the TFT (Fig. 5).

7. Claims 19-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirata in view of Sato.

As to claims 19-22: Hirata discloses an active matrix substrate for a liquid crystal display having a TFT, and a side light shielding layer (7) covering the

TFT. Sato teaches a first insulating layer having a stepped portion and a light shielding layer (10) covering the stepped portion and the partial removal (hole, CH).

Hirata, however, does not go into the details of the manufacturing method of the active matrix substrate.

Sato teaches a method of manufacturing the liquid crystal display panel.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to adapt the method of manufacturing the display as taught by Sato such that the display can be manufactured that contains all the features taught by both Hirata and Sato.

8. Claims 23 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirata and Sato as applied to claim 21 above, and further in view of Kim (U.S.Patent No. 6,587,165).

As to claims 23 and 24: Neither Hirata nor Sato disclose a second insulating layer or the flattening of the second insulating layer by chemical mechanical polishing.

Kim in disclosing a method of manufacturing semiconductor device capable of improving planarization, teaches the use of a second insulating layer (27) and a planarization process by chemical mechanical polishing (CMP) technique (col. 3, lines 30-35).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to adapt the chemical mechanical

polishing technique to planarize the second insulating layer as taught by Kim to the device of Hirata and Sato to achieve a high degree of integration of semiconductor devices and a low-temperature planarization process such as CMP (col. 1, lines 16-33).

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. (a) Fukata et al. (U.S.Patent No. 6,449,022) (b) Kobayashi et al. (U.S.Patent No. 5,847,792) and (c) Hashimoto (U.S.Patent No. 5,784,132).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Prasad R Akkapeddi whose telephone number is 571-272-2285. The examiner can normally be reached on 7:00AM to 5:30PM M-Th.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert H Kim can be reached on 571-272-2293. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Prasad R Akkapeddi, Ph.D
Examiner
Art Unit 2871

*** SRA

TARIFUR R. CHOWDHURY
PRIMARY EXAMINER